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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,880	08/10/2004	Louis C. Hsu	FIS920040114US1	4879

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EXAMINER
ANYA, IGWE U

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,880	HSU ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 2, 4 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Temple et al. (US Patent 5654226).

4. Temple et al. teach a method of manufacturing integrated circuit chips, comprising:

partially joining an integrated circuit wafer (10) to a supporting wafer (12) at a limited number of joining points (18);

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer (col. 2 line 62 – col. 3 line 2); and

cutting through said integrated circuit wafer to form chip sections (fig. 1 element 20-saw lines)

wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points (dicing line 20 overlaps joining points);

further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process (fig. 1);

wherein chip sections where the integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer (figs. 2);

wherein said joining process comprises a bonding process (col. 2 lines 62 – 66);

wherein said joining process comprises a thermal oxide bonding process (col. 3 lines 15 – 20); and

wherein said joining process creates said joining points to survive processing temperatures that are reached during said processing that forms said devices and said wiring in said integrated circuit wafer (col. 2 line 66 – col. 3 line 2).

5. Temple et al. lack a wafer with a planar surface and the oxide regions at the planar surface.

6. However, omission of an element and its function in a combination where the remaining elements perform the same function as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

7. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fill the gap with any none thermal bonding material including silicon.

8. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delgado et al. in view of Yoshihara et al. (US Patent 6555901).

9. Delgado et al. teach a method of manufacturing integrated circuit chips comprising:

partially joining an integrated circuit wafer to a supporting wafer at a limited number of joining points (figs. 1 element 22); reducing the thickness of said integrated circuit wafer (col. 3 lines 11 – 19 & figs. 1C, 1D);

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer (col. 3 lines 27 –31); and

cutting through said integrated circuit wafer to form chip sections, wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points (col. 3 lines 39 – 44 & fig. 1F);

further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process (fig. 1C);

wherein chip sections where said integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer (col. 4 lines 43 – 53 & fig. 5B);

wherein said joining process comprises a bonding process (col. 3 lines 11 – 19);

wherein said joining process comprises a thermal oxide bonding process(col. 3 lines 1 – 10);

wherein said joining process creates said joining points to survive processing temperatures that are reached during said processing that forms said devices and said wiring in said integrated circuit wafer (col. 3 lines 1 – 37); and

chemically-mechanically polishing said integrated circuit wafer to reduce the thickness of said integrated circuit wafer (col. 3 lines 22 – 24).

10. Delgado et al. lack the step further comprising:

before said joining process, roughening portions of said integrated circuit wafer facing said supporting wafer to create rough surface portions at the interface of said integrated circuit wafer, wherein said roughening process avoids producing rough surface portions adjacent said joining points; and

a wafer having a planar surface and segmented oxide regions planar with the surface.

11. However, Yoshihara et al. teach a method of roughening portions of said integrated circuit wafer facing said supporting wafer to create rough surface portions at the interface of said integrated circuit wafer, wherein said roughening process avoids producing rough surface portions adjacent said joining points before the joining process (col. 6 lines 54 – 65) to promote a eutectic reaction.

12. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yoshihara et al. into the Delgado et al. reference to enhance the bonding strength.

13. Regarding a wafer having a planar surface and segmented oxide regions planar with the surface, omission of an element and its function in a combination where the remaining elements perform the same function as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

Response to Arguments

14. Applicant's arguments filed 13 September 2005 have been fully considered but they are not persuasive. Prior art references teach selective bonding of wafers at oxide points, but lack a planar surface. However, any non-thermal bonding material may be used in filling the gaps without affecting the scope of prior art teachings. Furthermore, applicant has not disclosed planarizing the surface solves any stated problem, or is for any particular purpose, and the invention appears to perform equally well with prior art teachings.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2891

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER

IA

November 25, 2005